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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,425	10/02/2003	Robert A. Shearer	ROC920030170US1	8448

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

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07/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/677,425	SHEARER, ROBERT A.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-19 are pending in the Application.

Claims 20-22 are cancelled.

Claims 1 and 8 are amended.

Claims 1-19 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 29 May 2007 in response to the office action mailed on 28 February 2007 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller (US Patent 6,044,418) in view of Welch et al. (US Patent 6,735,633 B1) hereinafter Welch, and in further view of Mammen (US PG Publication 2004/0047367 A1).

As for claim 1, Muller teaches a memory device, comprising:

a buffer memory having a plurality of addressable memory registers (Fig. 4 illustrates a queue with multiple registers arranged into a plurality of section or partitions);

a logic network for writing and reading data into and out of said buffer memory (Fig. 1, element 101), said logic network for partitioning said buffer memory into a plurality of buffer regions (col. 1, line 54 through col. 2 line 1 – the system can dynamically change the number and sizes of queues (see Fig. 4, the queue is partitioned into at least two regions, elements 425 and 430)), wherein said logic network writes and reads data from a plurality of unique data classes into said plurality of buffer regions such that each data class is uniquely written into and uniquely read from a different buffer region col. 6, lines 26 through 34 – each of the partitions maintain data that is communicated through a corresponding network port. Additionally, the partitions can be either data or other information. In other words, each partition is capable of containing information or data unique to its corresponding network port (i.e. own class of data).

Muller however fails to teach a timer sending a timing signal to recall data from a counter and repartition the buffer. It is worthy to note that Muller does teach repartitioning the buffer such that a more utilized buffer region is assigned more addressable memory registers (col. 2, lines 9-12 - under and over utilization of the buffer regions is corrected via the resizing based on usage. In other words, assigning

more registers to region that require more memory, and less to those that are under utilization their respective allocated areas).

Welch however teaches a system for bandwidth allocation in a computer network where a timer is used to time when resource reallocation is required. Once the timer is reset, it will increment between reallocation requests (col. 14, lines 21-24). Once reallocation is required the timer sends a signal to the system to indicate that reallocation is required (col. 14, lines 55-64). Subsequently, the timer will then be cleared (i.e. recalling data from the timer, which has served as a counter for the interval between reallocation (col. 14, lines 42-54)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Welsh's system for bandwidth allocation to is own system. By doing so Muller would benefit by improving the bandwidth of his own network, thereby minimizing possible data loss during packet transmissions as discussed by Welsh in col. 2, lines 12-24.

It is worthy to note that even though Muller is teaching memory allocation, and Welsh's system is for resource (i.e. bandwidth) reallocation, Welsh's system is analogous to Muller's, in that they both serve to reallocate resources over a network fabric. Welsh's teachings are introduced to show that adding a timing signal to trigger Muller's memory reallocation is an obvious variation of his presently taught system.

Muller further fails to teach incrementing a storage register every time a region reaches a predetermined usage level.

Mammen however teaches a method and system for optimizing the size of a variable buffer in which he maintains buffer read and buffer write pointers used determine if a buffer region is full. If it is determined that the buffer is full, a counter is incremented to indicate to the system that the buffer is now full (paragraph 0084, lines 17-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Mammen's system for optimizing the size of a buffer. By doing so, Muller would benefit by having a means of more effectively minimizing the depth of the buffer in his network, which in turn would produce a low delay in message transmission, hence reducing the possibility of future underflow due to packet delay variations as taught by Mammen (paragraph 0006, all lines).

As for claim 2, Muller teaches the logic network as assigning a buffer region that is used less often fewer addressable memory registers (col. 2, lines 9-12 - under and over utilization of the buffer regions is corrected via the resizing based on usage. In other words, assigning more registers to region that require more memory, and less to those that are under utilizing their respective allocated areas).

As for claim 3, Muller teaches each buffer region is always assigned at least a minimum number of addressable memory registers (this limitation is inherent as a region must contain at least one register or storage location to be considered a valid region, therefore the minimum number of addressable registers per region is always one).

As for claim 4, Mammen teaches a method and system for optimizing the size of a variable buffer in which he maintains buffer read and buffer write pointers used determine if a buffer region is full. If it is determined that the buffer is full, a counter is incremented to indicate to the system that the buffer is now full (paragraph 0084, lines 17-24). In other words, the predetermined level is set to full as claimed by Applicant.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Mammen's system for optimizing the size of a buffer. By doing so, Muller would benefit by having a means of more effectively minimizing the depth of the buffer in his network, which in turn would produce a low delay in message transmission, hence reducing the possibility of future underflow due to packet delay variations as taught by Mammen (paragraph 0006, all lines).

As for claim 5, Muller teaches a least used buffer region is assigned the minimum number of addressable memory registers the logic network assigns a buffer region that is less often fully utilized but that has more than the minimum number of addressable memory registers (again, a memory region will always contain at least one register (minimum), yet it will always allocate more to accommodate future writes into the region).

As for claim 7, Welch teaches resetting the timer (i.e. counter) after the reallocation occurs (col. 14, lines 42-54).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Welsh's system for bandwidth allocation into his own system. By doing so Muller would benefit by improving the

bandwidth of his own network, thereby minimizing possible data loss during packet transmissions as discussed by Welsh in col. 2, lines 12-24.

4. Claims 6 and 8-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Muller (US Patent 6,044,418), Welch (US Patent 6,735,633 B1) and Mammen (US PG Publication 2004/0047367 A1), and in further view of Gil (US PG Publication 2004/0064664 A1).

As for claim 8, the combined teachings Muller, Welch and Mammen meet all of the limitations of this claim with the exception of a card adaptor for transmitting and receiving data from the network switch (see the rejection of claim 1).

Gil however teaches a buffer management architecture and method for an Infiniband subnetwork. In his teachings, Gil discloses Infiniband architecture HCA card adapter in his network (paragraph 0003, all lines – see also Fig. 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Muller, Welch and Mammen to further include Gil's buffer management architecture. By doing so, their combined teachings would be able to exploit the benefits of an Infiniband type architecture including improved bandwidth and lower data latency over the network as described by Gil (paragraph 0003, all lines).

Claims 9-12, and 14 are similar to claims 1-5, and 7, and hence are rejected with the same rational.

As for claims 6 and 13, though Muller teaches each buffer region as storing data or information (i.e. data classes) unique to each port, he fails to specifically teach the classes as representing virtual lanes. Gil however teaches the use of virtual lanes for the ports for the HCA (paragraph 0005, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Muller, Welch and Mammen to further include Gil's buffer management architecture into his own system of dynamically resizing queues for a network switch. By doing so, their combined teachings would be able to exploit the benefits of an Infiniband type architecture including improved bandwidth and lower data latency over the network as described by Gil (paragraph 0003, all lines).

As for claim 17, Gil teaches his card adaptor as a target adaptor (paragraph 0004, all lines).

As for claims 15-16 and 18-19, Gil teaches his card adaptor as a Infiniband host channel adaptor (paragraph 0005, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Muller, Welch and Mammen to further include Gil's buffer management architecture into his own system of dynamically resizing queues for a network switch. By doing so, their combined teachings would be able to exploit the benefits of an Infiniband type architecture including improved bandwidth and lower data latency over the network as described by Gil (paragraph 0003, all lines).

Response to Arguments

5. Applicant's arguments with respect to claims 1-19 have been fully considered, but they are not persuasive.

Applicant asserts, "the references, even when combined as suggested in the *Office Action,* fail to teach the use of a logic network that "writes and reads data from a plurality of unique data classes into said plurality of buffer regions such that each data class is uniquely written into and uniquely read from a different buffer region," as recited in independent claims 1 and 8." Applicant concludes, "none of the references teaches the assignment of each network's data to a corresponding and separate data class, much less the separate and unique storage of each data class in its own portion of the data buffer memory space, as recited in the claims."

This argument however is not persuasive. Examiner maintains that Muller does in fact teach the logic network as writing and reading data from a plurality of data classes into different buffer regions - col. 1, line 54 through col. 2, line 1 and col. 6, lines 26-34. Unique sets of data and information are stored into separate buffer regions in order to enable the partition to store information or data unique to its corresponding network port (i.e. class of data). The class data stored is in fact "uniquely written into" and "uniquely read from", Applicant's arguments notwithstanding. Since Applicant has not explicitly defined writing and reading data "uniquely", Examiner must turn to extrinsic evidence in order to ensure the term is given its "broadest reasonable interpretation consistent with Applicant's specification", pursuant to MPEP § 2111. Examiner asserts that "uniquely" may be broadly construed as "limited in occurrence to a given class,

situation, or area". Since Muller clearly teaches storing the data unique to a respective port in different areas (i.e. partitions – Fig. 4, elements 425 and 430), Muller inherently writes data into, and reads data from the buffers "uniquely".

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

7. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

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SUPERVISORY PATENT EXAMINER
7/25/07